AND8240

Designing NCP1381 and NCP1382 in High Power AC-DC Adapters

Nicolas Cyr
ON Semiconductor

ON Semiconductor®

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The NCP1381 and NCP1382 are valley−switching controllers offering various features making it ideal to build efficient High Power AC−DC adapters. For instance, it has the capability to control the activity of the Power Factor Correction (PFC) front stage that highly simplifies PFC implementation. More generally, the NCP1381/82 incorporates all the major up−to−date functions (most of them programmable) to ease the optimization of any specific application and the compliance to the specifications of modern power supplies, including reliability and standby efficiency.

Main features

- ***Current−Mode Operation with Quasi−Resonant Operation:*** Implementing peak current mode control, NCP1381/82 waits until the voltage across the external switching device crosses a minimum level. This is the quasi−resonance approach, minimizing both EMI radiations and capacitive losses.
- ***Over Power Protection:*** Using a current image of the bulk level (via the brown−out divider), it is easy to create an offset on top of the current sense information by inserting a series resistor, providing an efficient line compensation method.
- ***Frequency Clamp:*** The controller monitors the sum of t_{ON} and t_{OFF}, providing a real frequency clamp. Also the t_{ON} maximum duration is safely limited to 45 μs in case the peak current information is lost. If the maximum t_{ON} limit is reached, then the controller stops all pulses and enters a safe auto−recovery burst mode.
- ***Blanking Time:*** to prevent false tripping with energetic leakage spikes, the controllers includes a 3 μs blanking time after the T_{OFF} event.
- ***Go−to−Standby Signal for PFC Front Stage:*** NCP1381/82 includes an internal low impedance switch connected between Pin 10 (V_{CC}) and Pin 11 (GTS). The signal delivered by Pin 11 being of low impedance, it becomes possible to connect PFC's V_{CC} directly to this pin and thus avoid any complicated interface circuitry between the PWM controller and the PFC front−end section. In normal operation, Pin 11 routes the PWM auxiliary V_{CC} to the PFC circuit which is thus directly supplied by the auxiliary winding. When the SMPS enters skip−cycle at low output power levels, the controller detects and confirms the presence of the skip activity by monitoring the signal applied on its pin ADJ_GTS (typically a portion of FB signal) and opens Pin 11, shutting down the front−end PFC stage. When this signal level increases, e.g. when the SMPS goes back to a normal output power, Pin 11 immediately (without delay) goes back to a low impedance state. Finally, in short−circuit conditions, the PFC is disabled to lower the stress applied to the PWM main switch.
- ***Low Startup−Current:*** Reaching a low no−load standby power represents a difficult exercise when the controller requires an external lossy resistor connected to the bulk capacitor. Due to a novel silicon architecture, the startup current is guaranteed to be less than 15 μA maximum, helping to reach a low standby power level.
- ***Skip−Cycle Capability:*** A continuous flow of pulses is not compatible with no−load standby power requirements. Slicing the switching pattern in bunch of pulses drastically reduces overall losses but can, in certain cases, bring acoustic noise in the transformer. Due to a skip operation taking place at low peak currents only, no mechanical noise appears in the transformer. This is further strengthened by ON Semiconductor soft skip technique, which forces the peak current in skip to gradually increase. In case the default skip value would be too large, connecting a resistor to the Pin 6 will reduce or increase the skip cycle level. Adjusting the skip level also adjusts the maximum switching frequency before skip occurs.
- **Soft−Start:** A circuitry provides a soft−start sequence which precludes the main power switch from being stressed upon startup. This soft−start is internal and reaches 5 ms typical.

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- **Overvoltage Protection:** By sensing the plateau level after the power switch has opened, the controller can detect an over voltage condition through the auxiliary reflection of the output voltage. If an OVP is sensed, the controller stops all pulses and permanently stays latched until the V_{CC} is cycled down below 4 V.
- ***External Latch Input:*** By permanently monitoring Pin 5, the controller detects when its level rises above 3.5 V, e.g. in presence of a fault condition like an OTP. This fault is permanently latched−off and needs the V_{CC} to go down below 4 V to reset, for instance when the user un−plugs the SMPS.
- ***Brown−Out Detection:*** By monitoring the level on pin 2 during normal operation, the controller protects the SMPS against low mains condition. When the Pin 2 level falls below 240 mV, the controllers stops pulsing until this level goes back to 500 mV to prevent any instability. During brown−out conditions, the PFC is not activated.
- ***Short−Circuit Protection:*** Short−circuit and especially over−load protection is difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the auxiliary winding level does not properly collapse in presence of an output short−circuit). In NCP1381/82, every time the internal 0.8 V maximum peak current limit is activated, an error flag is asserted and a time period starts, due to an external timing capacitor. If voltage on the capacitor reaches 4 V (after 90 ms for a 220 nF capacitor) while the error flag is still present, the controller stops the pulses and goes into a latchoff phase, operating in a low−frequency burst−mode. As soon as the fault disappears, the SMPS resumes its operation. The latchoff phase can also be initiated, more classically, when V_{CC} drops below VCC_{min} (10 V typical).

Typical Application

The above features makes NCP1381/82 well suited for medium to high power offline applications. Its typical application is a 75 W to 200 W AC−DC power supply such as a notebook adapter.

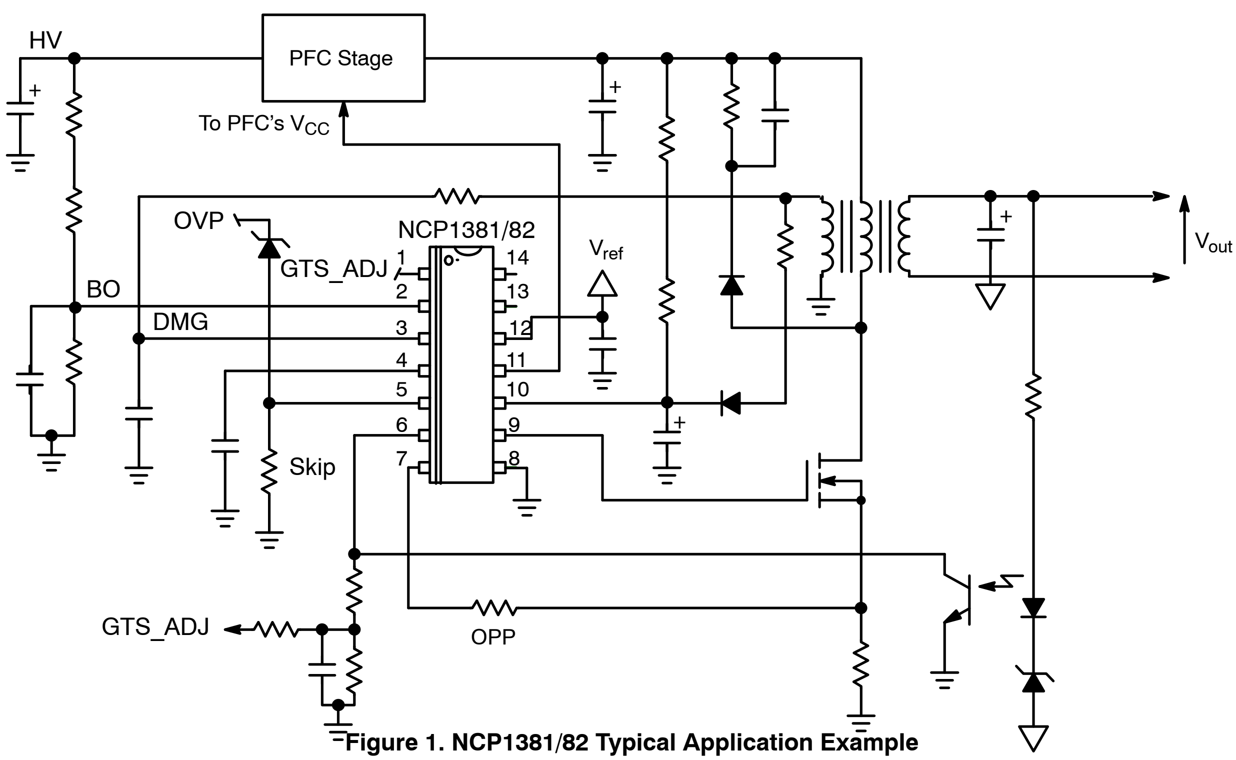

Figure 1. NCP1381/82 Typical Application Example

PIN−BY−PIN IMPLEMENTATION

Pin 1: “ADJ_GTS” Pin

This pin offers a comparator with adjustable hysteresis to define the turning ON and OFF conditions of the PFC controller. It is primarily intended to be connected to a portion of the FB voltage, but any other signal could be used as well (such as a rectified and averaged image of the DRV pin for instance). The purpose is to define the output power level at which the front−end PFC turns ON and OFF, in order to reduce the standby consumption of the application.

It consists in a simple comparator with fixed 250 mV reference: when the voltage applied on the pin is higher than 250 mV, GTS signal can turn on; and when it is lower than 250 mV, GTS signal is low. Additionally, when output of the comparator is high an internal current source delivers 5 μA to the pin, allowing the creation of an offset on top of the signal applied: as this offset disappears when the comparator turns off, it plays the same role as an hysteresis.

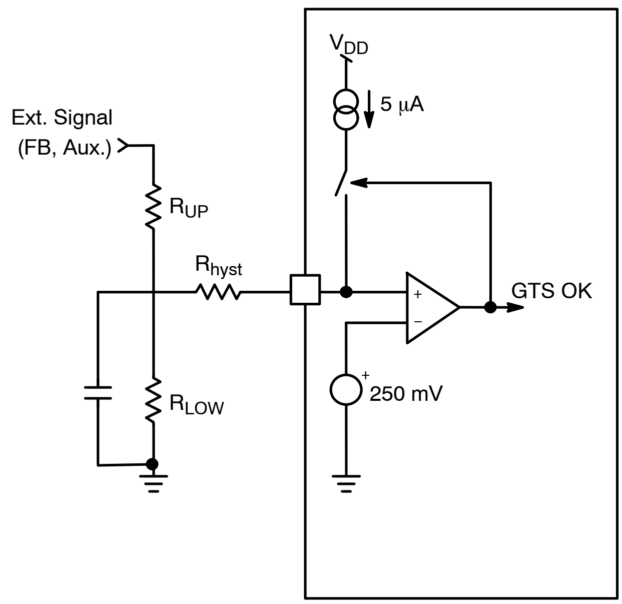

Figure 2. Internal Configuration of ADJ_GTS Pin

Design Steps (Considering R_{HYST} = 0)

- Choose the input signal levels at which GTS must turn on and off: V_{ON} and V_{OFF}
- Find the division ratio of the input resistor divider based on the turn−on level (case where the internal 5 μA current source is off):

$$\eta = \frac{0.25}{V_{ON}} \qquad \text{(eq. 1)}$$

- Find the equivalent resistance seen from the pin according to the turn−off level (case where the internal 5 μA current source is on):

$$0.25 = \eta \cdot V_{OFF} + 5 \cdot 10^{-6} \cdot R_{EQ}$$

$$\Rightarrow R_{EQ} = \frac{0.25 - \eta \cdot V_{OFF}}{5 \cdot 10^{-6}} \qquad \text{(eq. 2)}$$

Knowing that

$$\eta = \frac{R_{LOW}}{R_{UP} + R_{LOW}}, \text{ and } R_{EQ} = \frac{R_{UP} \cdot R_{LOW}}{R_{UP} + R_{LOW}},$$

it may be deduced

$$R_{UP} = \frac{R_{EQ}}{\eta} = 2 \cdot 10^5 \cdot (V_{ON} - V_{OFF}) \text{ and } R_{LOW} = \frac{\eta}{1 - \eta} \cdot R_{UP} = 5 \cdot 10^4 \cdot \frac{(V_{ON} - V_{OFF})}{(V_{ON} - 0.25)} \qquad \text{(eq. 3)}$$

- An additional constraint if the signal used is FB, is that $R_{UP} + R_{LOW}$ must be greater than 20 kΩ in order not to disturb FB behavior. If a smaller value is obtained, restart calculations with different V_{ON} and V_{OFF}.

Pin 2: "BO" Pin

SMPS are designed for a given input range. When the input voltage is too low, the power supply tends to compensate by sinking more current from the line to deliver the same output power. As a result, the power components may suffer from an excessive heating and ultimately the SMPS may be destroyed. Another consequence is that as when the electricity network weakens, its voltage tends to decrease, and as in this case SMPS tend to sink more current, electricity network gets weaker and weaker and eventually collapses (it is the reason why this protection is called 'brown−out' protection).

A simple solution to protect at the same time the power supply and the network is to stop the SMPS controller when the input voltage is too low. For this purpose Pin 2 offers a comparator with hysteresis able to stop the controller if the voltage applied is too low. By applying an image of the input voltage on the pin, it becomes possible to authorize operation above a certain level of mains only. The controller monitors this voltage and when the Pin 2 voltage is too low (i.e., when V_{pin2} is below 240 mV), the controller stops pulsing and keeps disabled until this level exceeds 500 mV. The 260 mV hysteresis prevents the instabilities that could result from the input voltage ripple. The brown−out protection is not latched: when the input voltage (V_{IN}) is below the target, the controller stops pulsing but it recovers operation as soon as (V_{IN}) goes back within the acceptable range.

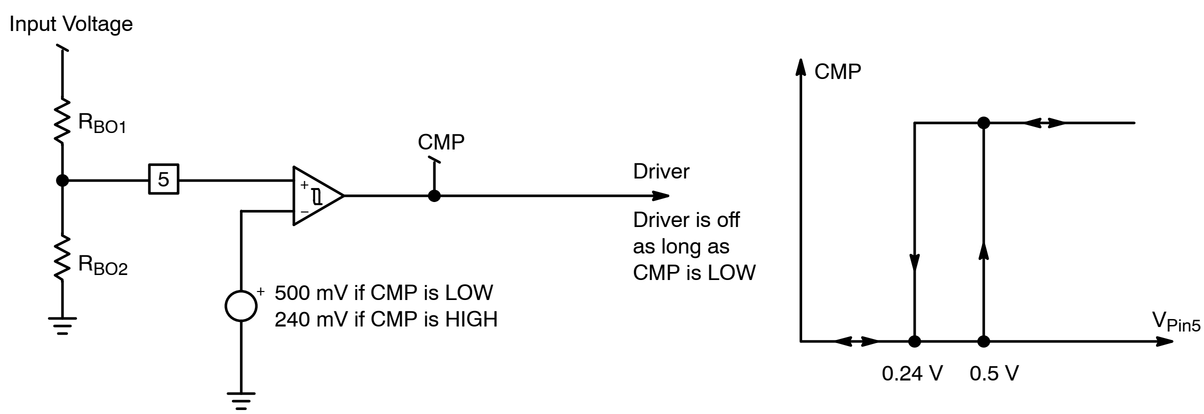

Figure 3. Internal Configuration of BO Pin

Which Input Voltage Should be Monitored?

- The PFC stage output voltage (“V_{BULK}” – bulk voltage).
- “V_{SIN}”, the PFC stage input voltage.

Figures 4 and 5 depict the two techniques.

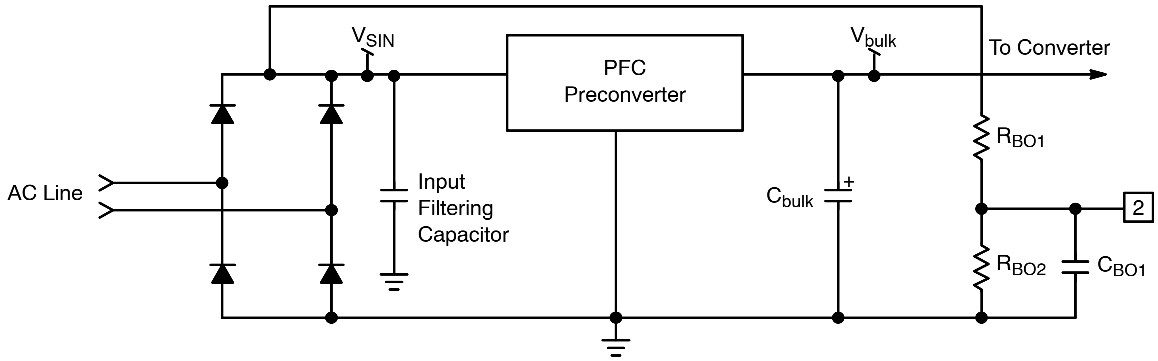

Figure 4. Brown–Out Detection on V_{SIN}

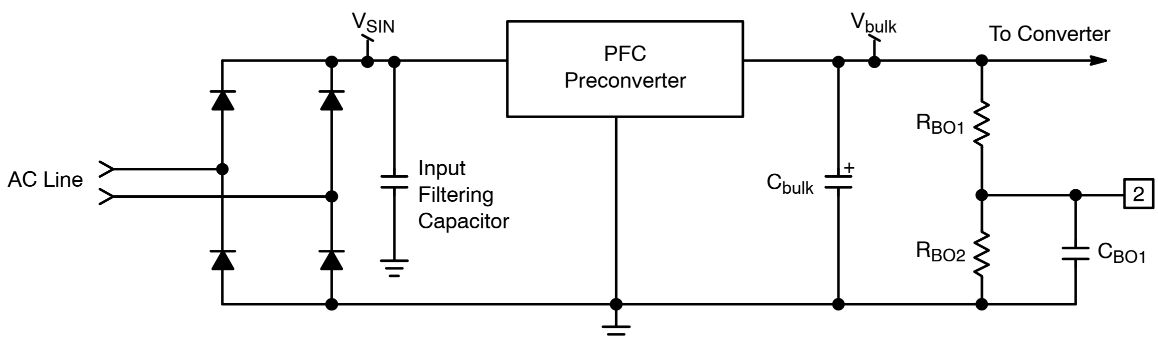

Figure 5. Brown–Out Detection on V_{BULK}

We will focus on V_{SIN} monitoring as this solution protects both PFC and SMPS stages. Figure 6 depicts V_{SIN} behavior when PFC stage starts.

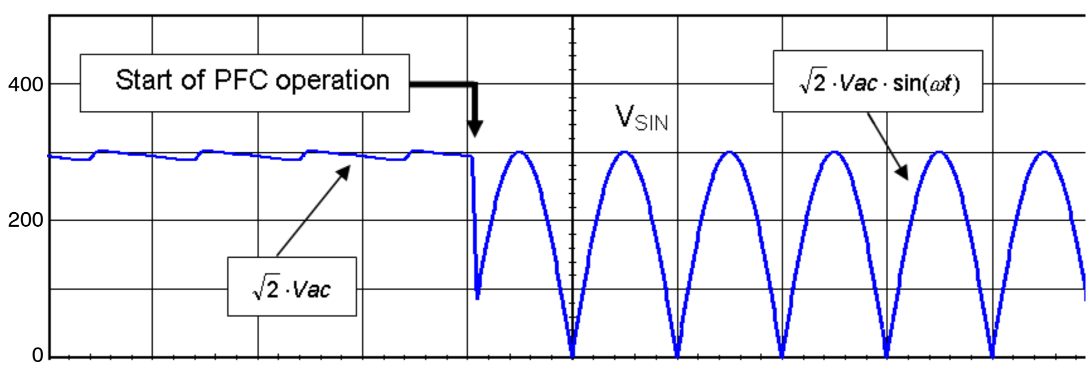

Figure 6. Voltage Across the Input Diodes Bridge (V_{SIN}) at PFC Startup

We clearly see two phases:

- The input voltage V_{SIN} is a substantially constant voltage when the PFC stage is off. The input bridge acting as a peak detector, the input voltage is flat and equates the AC line amplitude:

$$V_{IN} = \sqrt{2} \cdot V_{AC} \qquad \text{(eq. 4)}$$

Where V_{AC} is the RMS voltage of the line. Hence, the voltage applied to BO pin is:

$$V_{BO} = \sqrt{2} \cdot V_{AC} \cdot \frac{R_{BO2}}{R_{BO1} + R_{BO2}} \qquad \text{(eq. 5)}$$

This is the situation anytime when the PFC stage is off.

- The input voltage V_{SIN} is a rectified sinewave when the PFC stage operates. If C_{BO1} is large enough to suppress the AC component of BO voltage, pin 2 voltage is the following portion of the average value of V_{SIN}:

$$V_{BO} = \frac{2 \cdot \sqrt{2} \cdot V_{AC}}{\pi} \cdot \frac{R_{BO2}}{R_{BO1} + R_{BO2}} \qquad \text{(eq. 6)}$$

i.e. about 64% of the previous value. Therefore, the same line magnitude leads to a BO voltage that is 36% lower when the PFC is working compared to the pin 2 level when it is off. That is why the NCP1381/82 features a 48% hysteresis (V_{BOlow} = 0.48 x V_{BOhigh}). When the PFC stage starts operation, the input voltage equates the AC line peak. That is why the initial threshold of the brown−out comparator is its upper one ($V_{BO} = V_{BOhigh}$ = 500 mV when the NCP1381/82 starts operation).

Design Steps:

R_{BO1} and R_{BO2} can be calculated by using the following procedure:

1. Fix the current drawn by R_{BO1} and R_{BO2} so that it is compatible with the standby requirements. For instance, choose 50 μA consumed when V_{BO} reaches the 500 mV V_{BOhigh} threshold.
2. Evaluate R_{BO2} by:

$$R_{BO2} = \frac{0.5}{50 \cdot 10^{-6}} = 10\ \text{k}\Omega \qquad \text{(eq. 7)}$$

3. Calculate R_{BO1} by:

$$V_{BO} = \frac{2 \cdot \sqrt{2} \cdot VAC}{50 \cdot 10^{-6}} \approx \frac{\sqrt{2} \cdot V_{AChigh}}{50 \cdot 10^{-6}} \qquad \text{(eq. 8)}$$

Where V_{AChigh} is the AC line RMS voltage above which the circuit enters operation. For instance, if the desired threshold is 85 Vac, R_{BO1} = 2.39 MΩ.

The threshold at which the power supply stops (V_{AClow}) depends on the capacitor C_{BO1}.

If C_{BO1} is infinite, it fully suppresses the AC component of the input voltage portion that is monitored. Hence, V_{BO} is proportional to the average of the rectified AC line voltage:

$$V_{BOlow} = \frac{2 \cdot \sqrt{2} \cdot V_{AClow}}{\pi} \cdot \frac{R_{BO2}}{R_{BO1} + R_{BO2}} \Rightarrow V_{AClow} = \frac{\pi \cdot V_{BOlow}}{2 \cdot} \cdot \frac{R_{BO1} + R_{BO2}}{\sqrt{2} \cdot R_{BO2}}. \qquad \text{(eq. 9)}$$

$$\text{As } V_{AChigh} = V_{BOhigh} \cdot \frac{R_{BO1} + R_{BO2}}{\sqrt{2} \cdot R_{BO2}} \text{ we can deduce, i.e. } V_{AClow} = \frac{\pi}{2} \cdot \frac{B_{BOlow}}{V_{BOhigh}} \cdot V_{AChigh,} \text{ i.e.}$$

$V_{AClow} = V_{AChigh}$ x 75.4%. That means that if V_{AChigh} = 85 V, V_{AClow} = 64 V.

If V_{AClow} is too low, reducing C_{BO1} will increase the ripple injected to BO pin, and as a result decrease the hysteresis.

Using a simple simulation circuit (as proposed in Figure 7) rapidly gives the right value for C_{BO1} and the desired V_{AClow}. The simulation result of Figure 8 gives the V_{BO} ripple as a function of C_{BO1} in the case where:

$$V_{SIN} = \sqrt{2} \cdot 80 \sin(\omega \cdot t) \qquad \text{(eq. 10)}$$

To the light of this study, C_{BO1} = 470 nF is the capacitance necessary to have V_{AClow} = 80 V.

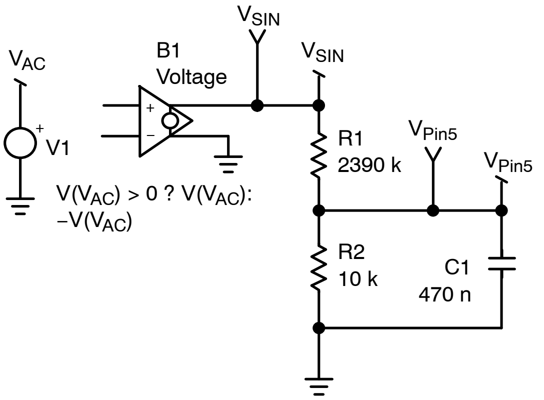

Figure 7. Brown−Out Detection Simulation Circuit

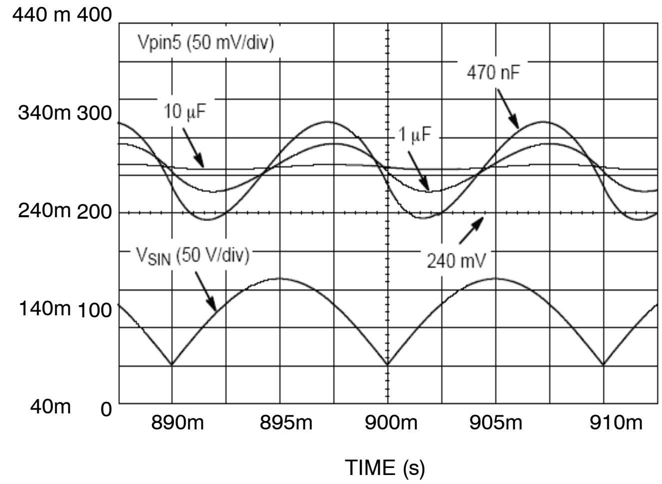

Figure 8. Results of the Simulation for Circuit of Figure 7

Without simulation tools, the procedure consist in implementing a large C_{BO1} value (leading to a time constant $R_{BO2} \cdot C_{BO1}$ in the range of 20 ms in 50 Hz or 60 Hz line conditions) and decreasing it until V_{AClow} reaches the wished value.

To Summarize

- Select R_{BO2} in the range of 10 kΩ (in order to limit the leakage current generated by the brown−out sensing network around 50 μA).
- Compute:

$$R_{BO1} = R_{BO2} \cdot \left(\frac{\sqrt{2} \cdot V_{AChigh}}{0.5} - 1 \right) \qquad \text{(eq. 11)}$$

- Implement C_{BO1} so that ($R_{BO2} \cdot C_{BO1}$) is in the range of 20ms. Then measure V_{AClow} and adjust C_{BO1} until V_{AClow} has the right value, knowing that reducing C_{BO1} increases V_{AClow}.

We will see later that Overpower Protection is dependent on V_{BO} voltage: to have an accurate protection, V_{BO} should be proportional to the input voltage of the SMPS stage, i.e. V_{BULK}. But once PFC has started, V_{BULK} is not any more an image of the mains voltage: it means that even if V_{SIN} goes below V_{AClow}, PFC stage will still try to maintain V_{BULK} high, and the brown−out protection is not effective. So connecting V_{BO} to V_{SIN} is recommended, even if overpower protection is less accurate. A solution to improve this protection is to use a “follower boost” type of PFC in which the output follows the input.

Pin 3: “DMG” Pin

In order to perform valley switching operation, NCP1381/82 monitors an auxiliary winding that gives an image of the voltage appearing on the drain of the switching MOSFET (Figure 9). Each time the decreasing voltage on DMG pin crosses 0 V, an internal comparator gives a clock signal to the internal latch that delivers the gate signal for the switching MOSFET (Figure 10).

The signal applied on DMG pin must be lower than 3.7 V in order not to activate the overvoltage protection, and the current flowing in the negative clamping protection diode must be kept below 3 mA. Internal circuitry is depicted in Figure 11.

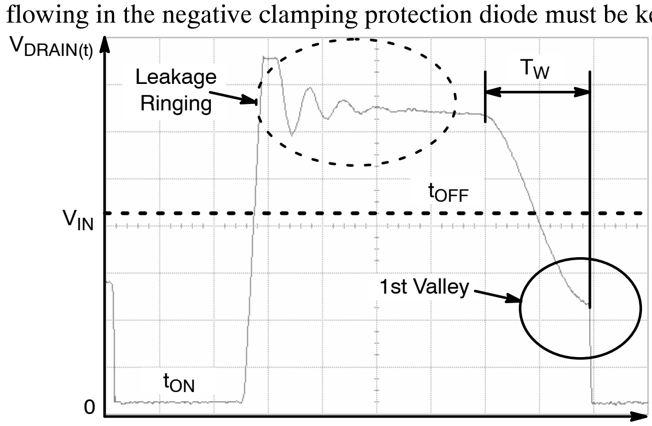

Figure 9. Voltage Appearing on the Drain of the Switching MOSFET

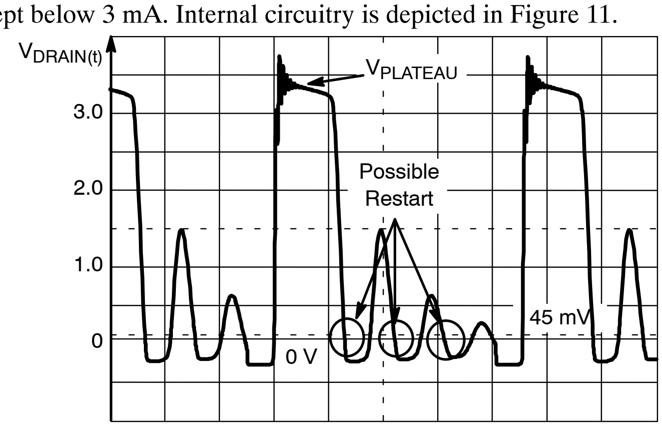

Figure 10. Corresponding Voltage Appearing on Pin DMG

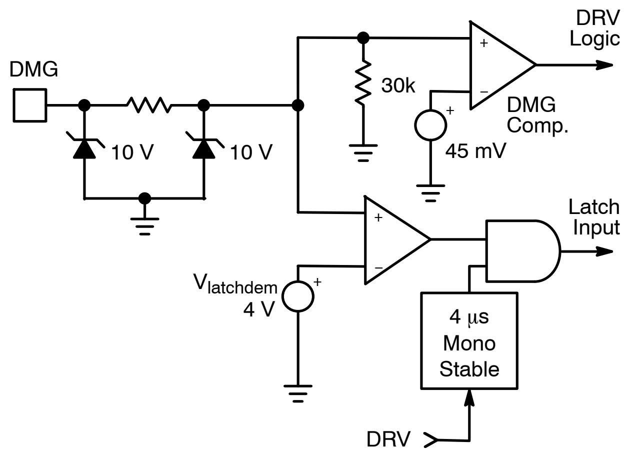

Figure 11. Internal Circuitry of DMG Pin

Design Steps:

- Knowing the plateau voltage $V_{PLATEAU}$ appearing on the auxiliary winding, calculate R_{DMG} taking into account the internal 30 kΩ pulldown resistor:

$$R_{DMG} \geq 3 \cdot 10^4 \cdot \frac{V_{PLATEAU} - 3.7}{3.7} \quad \text{(eq. 12)}$$

Verify that the current flowing through R_{DMG} when ESD clamping diode is activated (+10 V during t_{OFF}, −0.7V during t_{ON}) is within specification (+/−3mA). If not, choose R_{DMG} according to this maximum current, and then add an external resistor between DMG pin and ground (in parallel to the internal 30 kΩ resistor) to ensure V_{DMG} < 3.7 V during normal operation.

- Add a capacitor C_{DMG} between DMG pin and ground in order to delay the turn−on to the exact valley of the Drain signal. A first approximation for C_{DMG} consists in measuring the period of the oscillation (due to L_P the primary inductance and C_{DRAIN} the total capacitance on MOSFETs drain) appearing on the drain after demagnetization, or estimate it by:

$$T_{OSC} = 2 \cdot \pi \cdot \sqrt{L_P \cdot C_{DRAIN}} \quad \text{(eq. 13)}$$

The time T_{delay} between the zero crossing and the exact valley is one fourth this period, minus the roughly 200 ns inherent propagation delay of the controller:

$$T_{delay} = \frac{\pi}{2} \cdot \sqrt{L_P \cdot C_{DRAIN}} - 2 \cdot 10^{-7} \quad \text{(eq. 14)}$$

Eventually choose C_{DMG} so that ($R_{DMG} \cdot C_{DMG}$) is in the range of T_{delay}, and adjust it until the valley switching is correct.

Pin 4: "TIMER" Pin

The capacitor connected to this pin sets the duration of the fault timer, i.e. the delay after which the controller enters protection mode after detecting an overload condition. Its main purpose is to allow the cold startup (during which, by definition, the output is overloaded until the regulation level is reached), and to prevent any false triggering of the protection in a noisy environment. This timer is also used to prevent PFC shutoff during transient activation of the skip mode.

It is built around an internal 10 μA current source that charges the external capacitor until a 4 V comparator toggles (See Figure 12).

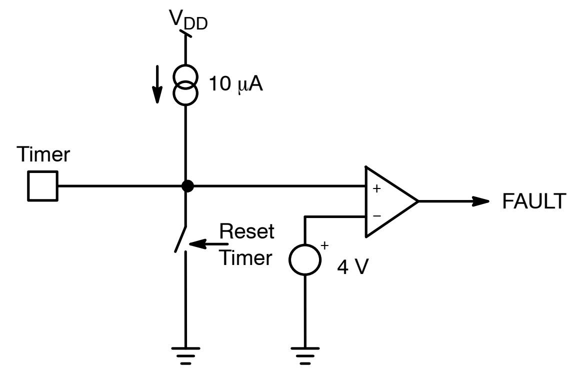

Figure 12. Internal Circuitry of TIMER Pin

Design Steps:

Once the V_{CC} capacitor is set (see V_{CC} section below), it gives the minimum time duration T_{FAULT} during which the controller must deliver power in overload condition during start−up. C_{TIMER} can then be estimated by:

$$C_{TIMER} \geq \frac{T_{FAULT} \cdot 10 \cdot 10^{-6}}{4}, \text{ i.e.}$$
$$C_{TIMER} \geq T_{FAULT} \cdot 25 \cdot 10^{-7}. \quad \text{(eq. 15)}$$

For instance if T_{FAULT} must be at least 80ms, C_{TIMER} should be greater than 200nF.

Pin 5: “SKIP / OVP” Pin

This pin performs two functions: it allows the setting of the FB pin level at which the controller starts to skip pulses in order to lower standby consumption, and at the same time provides a comparator to stop and latch the controller by any external condition (See Figure 13).

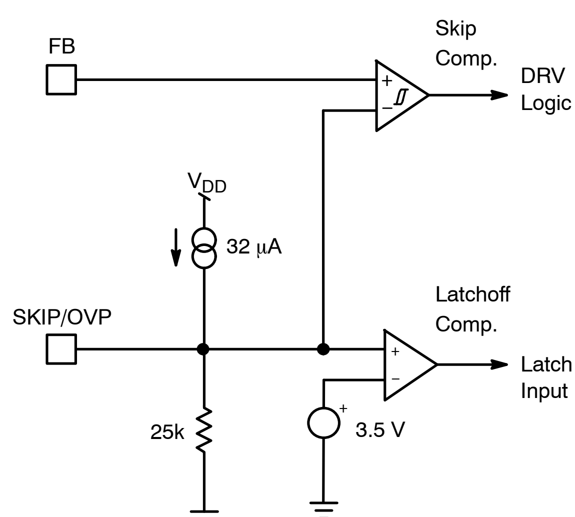

Figure 13. Internal Circuitry of Skip/OVP Pin

Design Steps:

- By default, skip level is set to 800 mV (32 μA through a 25 kΩ resistor), corresponding to 25% of maximum FB voltage (See FB Pin Section). Adding an external resistor to ground allows decreasing skip level, while adding a resistor from REF pin to Skip/OVP pin allows the increase of this level.
- This pin being at rather high impedance, it is necessary to add a filtering capacitor, which value depends on the amount of noise of the environment: a value from 100 nF to 1 μF is usually sufficient.
- To perform a latch function, the best way is to drive the REF signal to Skip/OVP Pin through an optocoupler or a simple bipolar transistor as exemplified in Figure 14.

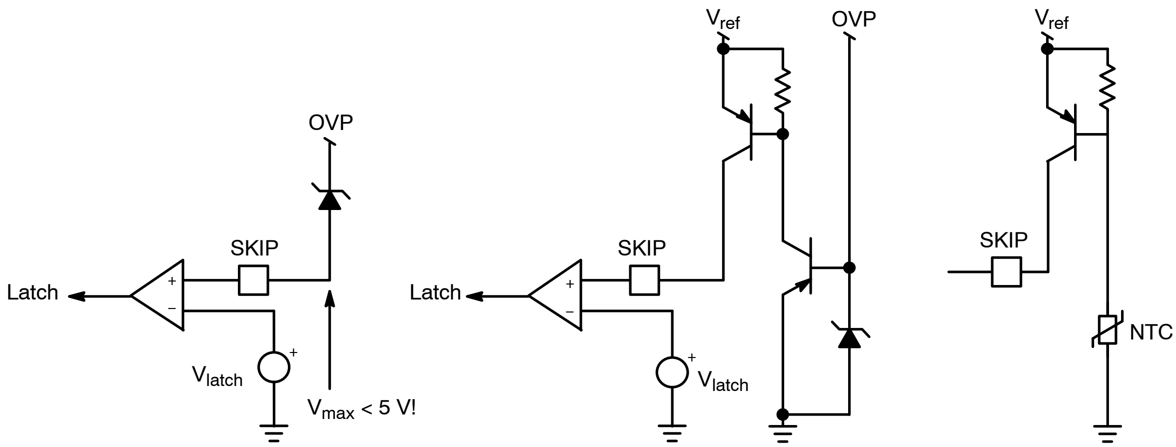

Figure 14. Possible use of the Latch Function of Skip/OVP Pin

Pin 6: "FB" Pin

The voltage on FB pin is divided by 4 and compared to CS Pin voltage to elaborate the t_{ON} duration (NCP1381/82 is a current−mode controller): it serves as a reference for the current sense comparator (See Figure 15). To simplify the connection of an optocoupler, an internal 10 kΩ pullup resistor is provided: optocoupler transistor can thus directly be plugged between FB pin and ground.

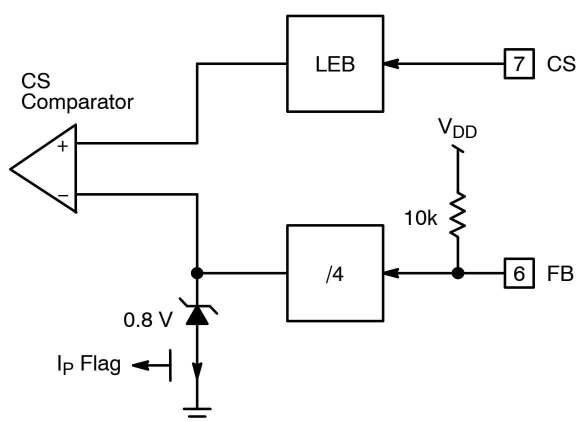

Figure 15. Internal Circuitry of FB Pin

Maximum CS pin voltage V_{CSmax} is 0.8 V, corresponding to a maximum FB voltage of 3.2 V: when voltage on FB pin is higher than 3.2 V, internal flag I_P flag is raised and fault timer is started. If $I_P$flag is still asserted when TIMER pin voltage reaches 4 V, FAULT is detected and the controller enters protection mode: pulses are stopped, and V_{CC} capacitor is discharged at a constant 1.4 mA current down to 7 V. Then a new start−up phase takes place, leading to a low−frequency burst mode safe for the power supply if the overload is still present. When the faulty condition disappears, the controller resumes normal operation after the next restart attempt (See Figure 16). If a resistive load is connected to FB pin (to generate ADJ_GTS signal for instance), it must be greater than 20 kΩ in order to allow the voltage on FB pin being greater than 3.2 V in overload conditions.

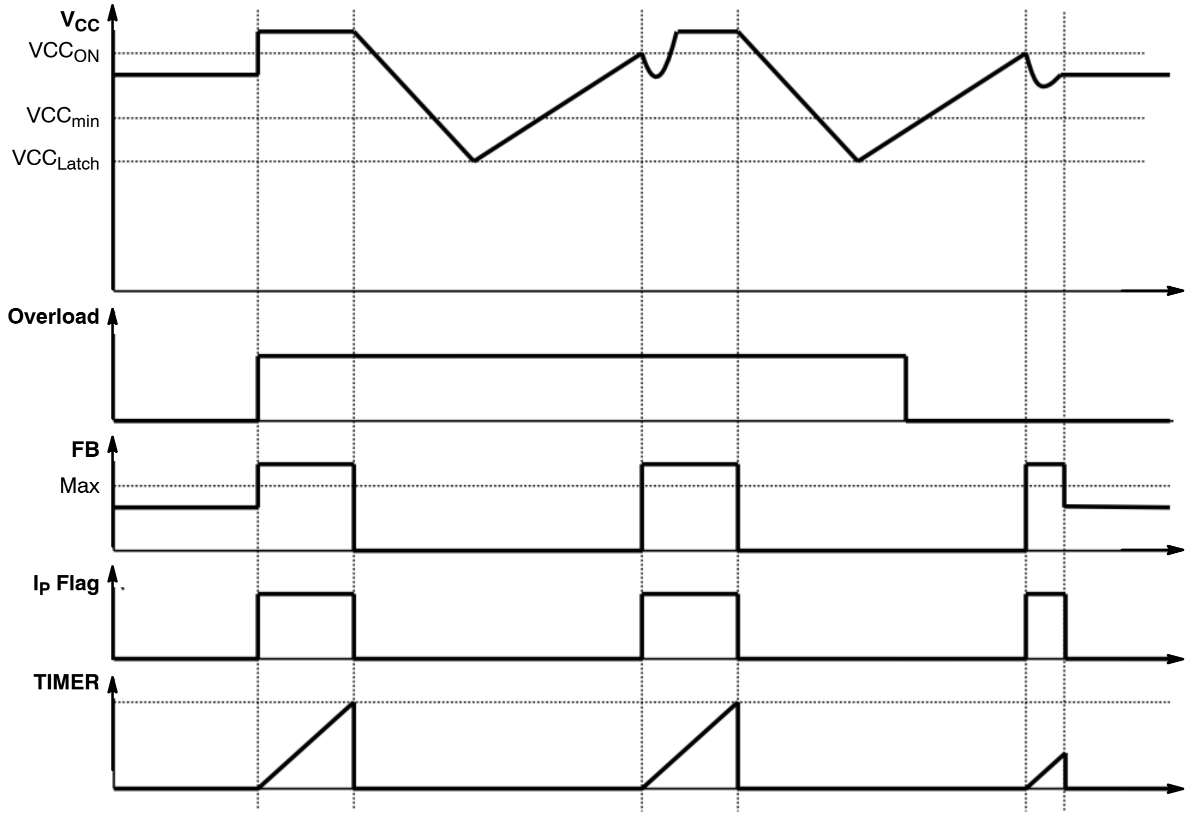

Figure 16. Typical Behavior in Overload Conditions

Pin 7: "CS" Pin

This pin performs two distinct functions: primary peak current reading and compensation for overpower protection.

Peak Current Reading

It is classically performed through the reading of the voltage appearing through a sense resistor connected between switching MOSFETs source and ground. The internal maximum current sense level V_{CSmax} is 0.8 V, so R_{SENSE} must be calculated by:

$$R_{SENSE} = \frac{0.8}{I_{pkmax}}, \quad \text{(eq. 16)}$$

With I_{pkmax} the maximum peak primary current at the lowest input voltage and maximum output load.

A leading edge blanking (LEB) prevents any spike appearing during the first 350 ns after t_{ON} to toggle falsely the internal current sense comparator. This LEB is usually enough, but if for some reasons an additional filtering is necessary, it is still possible to add externally an RC filter.

Overpower Compensation

In the quasi−resonant mode of operation, the slope of the current during ON time is ($V_{IN} \div L_P$), and is ($N \cdot V_{OUT}$) $\div$ (L_P) during OFF time. Thus for a given peak current I_{pk}, t_{ON} is shorter at high V_{IN} than at low V_{IN}, and t_{OFF} is constant: so the switching frequency F_{SW} is higher at high V_{IN} (See Figure 17).

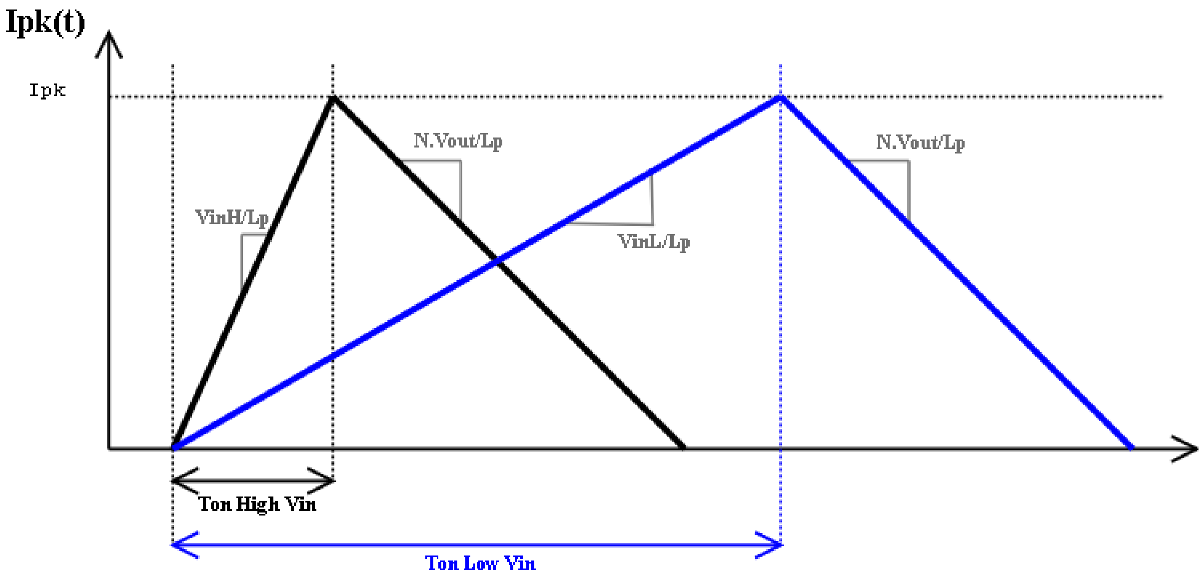

Figure 17. t_{ON} Behavior at a Given I_{pk} for Different V_{IN}

Knowing that:

$$P_{OUT} = \eta \cdot P_{IN} = \eta \cdot \frac{1}{2} \cdot L_P \cdot I_{pk}{}^2 \cdot F_{SW} \text{ (with } \eta \text{ the efficiency),} \quad \text{(eq. 17)}$$

It is clear that for a given I_{pk}, P_{OUT} is higher at high V_{IN} than at low V_{IN}. So for a constant output power, the peak current is lower at high V_{IN} than at low V_{IN} (See Figure 18).

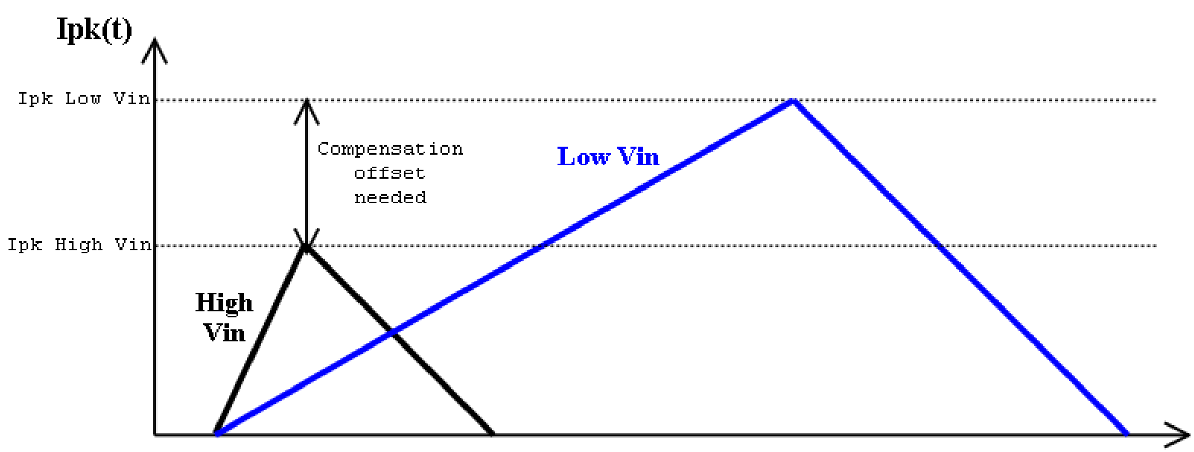

Figure 18. I_{pk} Behavior at a Given P_{OUT} for Different V_{IN}

As the overload detection of NCP1381/82 is based on peak current detection, if an overpower protection is needed the voltage applied on CS Pin at P_{OUTmax} must be the same at high V_{IN} and low V_{IN}. The solution consists in adding a compensation offset proportional to V_{IN} to the voltage sensed across the sense resistor. NCP1381/82 offers the possibility to easily create this offset by activating an internal current source proportional to V_{BO} during t_{ON}: this current flows out of pin CS and create an offset proportional to V_{BO} (which is proportional to V_{IN}) through a series resistor (See Figure 19).

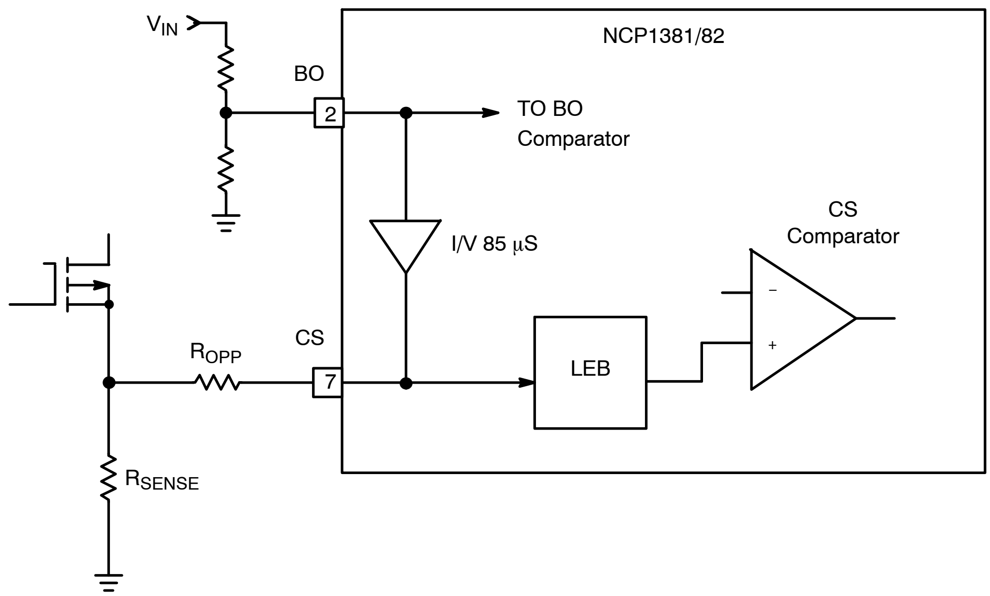

Figure 19. Internal Overpower Compensation Circuitry on CS Pin

Design Steps:

- Estimate peak current I_{pk} values at low V_{IN} and high V_{IN} for the maximum output power allowed. By neglecting the delay between core reset and the real valley (it is small compared to the switching period at high output power), we can estimate I_{pk} at a given V_{IN} by:

$$I_{pk} = \frac{2 \cdot P_{OUT}}{\eta} \cdot \left(\frac{1}{V_{IN}} + \frac{1}{N \cdot V_{OUT}}\right) \quad \text{(eq. 18)}$$

Thus calculate $I_{pkmaxLV}$ and $I_{pkmaxHV}$, respectively max peak currents at low and high input voltages.

- In the case where no offset is added, we saw that:

$$R_{SENSE} = \frac{0.8}{I_{pkmax}}$$

If an offset is added, we have at a given V_{IN}:

$$R_{SENSE} = \frac{0.8 - V_{offset}}{I_{pkmax}}$$

As we know what is the value of V_{BO} for a given V_{IN}, we can calculate

$$V_{offset} = R_{OPP} \cdot V_{BO} \cdot 85 \cdot 10^{-6}$$

Some lines of math eventually give:

$$R_{OPP} = \frac{0.8}{85 \cdot 10^{-6}} \cdot \frac{I_{pkmaxLV} - I_{pkmaxHV}}{V_{BOHV} \cdot I_{pkmaxLV} - V_{BOLV} \cdot I_{pkmaxHV}}$$

- Finally calculate R_{SENSE} by using:

$$R_{SENSE} = \frac{0.8 - R_{OPP} \cdot V_{BOLV} \cdot 85 \cdot 10^{-6}}{I_{pkmaxLV}} \quad \text{(eq. 19)}$$

Pin 8: “GND” pin

Reference ground for the controller.

Pin 9: “DRV” pin

By offering up to +500 mA/−800 mA peak, this pin allows to drive large Q_G MOSFETs without adding any additional components.

Pin 10: "V_{CC}" pin

This is the supply pin for the controller. It must be connected through a resistor to V_{BULK} for start−up supply, and to an auxiliary voltage for normal operation.

Design steps:

- Calculate V_{CC} capacitor: it must be able to supply the controller during start−up before the auxiliary voltage is high enough to take the hand, i.e. before the output reaches regulation. Startup V_{CC} voltage is 15 V, and minimum operating V_{CC} is 10 V: the maximum voltage drop on V_{CC} capacitor is thus 5 V. The current needed by the controller can be estimated by I_{CC1} (for NCP1381/82 internal supply) added to the current necessary to drive the switching MOSFET, given by the gate charge Q_G and the switching frequency F_{SW}:

$$I_{DRV} = Q_G \cdot F_{SW} \qquad \text{(eq. 20)}$$

To simplify the calculation, an average frequency of 60 kHz can be used as a rather good estimation. If we call T_{REG} the time before the output reaches regulation, V_{CC} capacitor must deliver $I_{CC1} + I_{DRV}$ during T_{REG} without dropping more than 5 V. Thus calculate:

$$C_{VCC} > \frac{(I_{CC1} + I_{DRV}) \cdot T_{REG}}{5} \qquad \text{(eq. 21)}$$

- Calculate the start−up resistor R_{START} in order to fulfil the start−up time (T_{START}) requirement:

$$T_{START} = \frac{C_{VCC} \cdot VCC_{ON}}{I_{START}} \qquad \text{(eq. 22)}$$

$I_{START} = (V_{BULK} - V_{CC}) \div (R_{START})$ is minimum at low V_{IN} when V_{CC} reaches VCC_{ON}, thus:

$$R_{START} < \frac{T_{START}}{C_{VCC}} \cdot \frac{V_{BULKmin} - VCC_{ON}}{VCC_{ON}} \qquad \text{(eq. 23)}$$

- Dissipated power in the start−up resistor at high input voltage is:

$$P_{START} = \frac{\left(V_{BULKmax} - VCC_{min}\right)^2}{R_{START}} \qquad \text{(eq. 24)}$$

This value will greatly contribute to the no−load standby power of the complete power supply. To reduce this wasted power, several possibilities exist, for instance: allow longer startup time, allow higher maximum output power to reach earlier output regulation, increase auxiliary voltage to supply V_{CC} before reaching regulation (but voltage on V_{CC} Pin must stay below 20 V).

A too big V_{CC} capacitor leads to a too long start−up time, or to a too high standby power. But it is sometimes needed to keep on supplying NCP1381/82 in no−load condition, where the power delivered by the auxiliary supply is very low. In this case, it is possible to have a separate tank capacitor, different from the V_{CC} capacitor (See Figure 20).

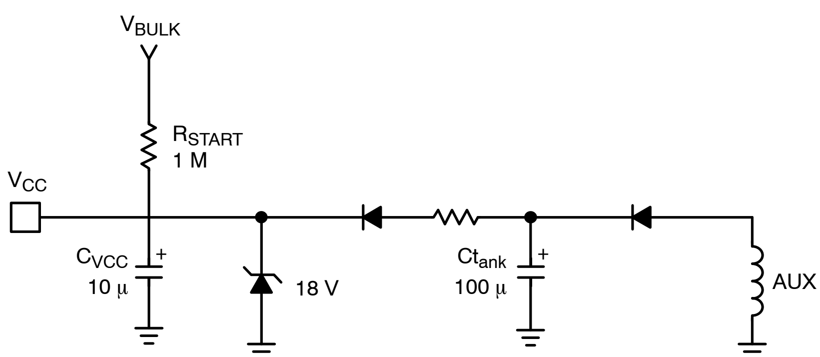

Figure 20. Split Capacitor on V_{CC} Pin

Pin 11: "GTS" Pin

V_{CC} is applied to GTS through an internal low−resistance switch. It is intended to be connected directly to supply pin of the front−end PFC controller.

Pin 12: "REF" Pin

A 5 V/10 mA reference voltage is available on pin REF. A filtering capacitor must be connected to this pin: 100 nF to 1 μF (depending on the noisiness of the environment) is usually enough.

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